REMARKS

The above amendments and these remarks are being submitted in response to the Final Office Action dated November 27, 2001, the teleconference with the Examiner on January 14, 2002 and the Advisory Action dated February 12, 2002, relating to the above-identified application.

I. Summary of the Examiner's Rejections/Objections

Claims 1-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Aleksic (U.S. Patent No. 5,914,722) in view of Lentz, et al. (U.S. Patent No. 5,446,836), and further in view of Wong, et al. (U.S. Patent No. 6,034,699).

II. Summary of the Applicant's Amendments

Claims 3-13 have been cancelled. Claims 1-2 and 14-15 have been amended. Claims 18-27 have been added.

III. Applicant's Response to the Examiner's Rejections

A. Prior Objection to the Drawings

The Applicants submitted drawing corrections for Examiner approval in response to a prior objection thereto. The Applicants wish to thank the Examiner for accepting and approving the proposed drawing corrections. The objection to the drawings was indicated to Applicants as being overcome during the January 14, 2002 telephone conference with the Examiner.

B. Rejection of Claims 1-3

By this Amendment, claim 3 has been cancelled. Thus, the Applicant's submit that the rejection of claim 3 is now moot.

The Applicants traverse the rejection of claims 1 and 2 for the reasons set forth below. The present invention is directed to a circuit and corresponding method for generating an optimal initial rasterization starting point estimate for a rasterizer (e.g. raster engine) to use when rendering an image. The initial rasterization starting point can be used to efficiently and quickly render a primitive by providing an appropriate raster engine with an initial scanning point that is substantially within or near the primitive. By employing the circuit and method of the present invention, the time for scanning and rendering a primitive is significantly shorter as compared to

conventional methods. The inventive method of the present invention is defined in claim 1 which calls for, among other things:

> "...generating region bits representing the location of the sorted vertex data with respect to a current tile being rendered;
> generating coordinate data representing an initial rasterization starting point estimate when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered and discarding the vertex data of primitives that lie outside the boundary of the current tile being rendered..."

In performing the aforementioned steps, the initial rasterization starting point of a primitive provided by the present invention is substantially within the current tile being rendered. Thus, the downstream rendering logic can be simplified as the sorted vertex data is provided in a predetermined manner and, additionally, the subsequent rendering time is reduced as the initial rendering point is substantially within the tile currently being rendered. Therefore, valuable processing time is not wasted finding a point within the primitive to be rendered. Such combination of steps and the benefits provided thereby are not taught or suggested by the combination of references as cited by the Examiner.

As understood, Aleksic is directed to a pixel scanning method used when a portion of an object being scanned crosses, or lies outside of a page boundary. The scanning of the object is described, for example, at col. 3, line 62-col. 4, line 10 (walk along each span, incrementing and x-coordinate of pixels along the span and decrementing the number of pixels making up the span). However, Aleksic is silent on how the initial scan point (e.g. the point to begin the edge and span walker processes) is generated. As Aleksic does not disclose how the initial scan point is generated, it therefore does not teach or suggest the aforementioned combination of steps as defined in claim 1.

In addition, adding the teachings of Lentz, et al. to the teachings of Aleksic will also not render the invention as defined in claim 1 obvious as Lentz, et al. does not overcome the aforementioned deficiency in Aleksic. In addition, Lentz, et al. also does not teach or suggest the aforementioned combination of steps performed to generate the initial reasterizaton starting point as defined in claim 1. As understood, Lentz, et al. is directed to a system and corresponding method for rendering polygons that incorporate a w-bit wide render mask to provide an indication of which bits along a scan line are to be subsequently rendered. *See*, for example, col. 6, lines 34-55. However, there is no teaching or suggestion of the generation or use of data

representing an "...initial rasterization starting point..." as defined in claim 1. In fact, Lentz, et al. expressly states that "methods for determining the order of traversal are not discussed here." (*See*, col. 9, lines 52-53). Thus, determining an initial rasterization starting point is not a consideration or requirement of Lentz, et al. To further augment this point, the Examiner's attention is directed to, for example, col. 10, lines 31-33, which states in pertinent part:

> "...[t]he traversal algorithm begins the scan at some pixel and determines the value of the edge variables based upon the functions above..."

However, Lentz, et al. is silent on how to determine the beginning scanning point. Consequently, as Aleksic does not disclose a method of generating an "...initial rasterization starting point..." based, in part, on region bits resulting from previously sorted vertex data and Lentz, et al. explicitly does not discuss the generation of an initial rasterization starting point (*see*, col. 10, lines 31-33), the combination of Aleksic and Lentz, et al. does not render the invention as defined in claim 1 obvious.

To overcome the shortcomings of the combination of Aleksic and Lentz, et al., the Examiner added the teachings of Wong, et al. to the combined teachings of Aleksic and Lentz, et al. and states that the combination thereof renders the claimed invention obvious. The Applicants traverse this ground of rejection and the addition of the Wong, et al. reference for the reasons set forth below. As understood, Wong, et al. is directed to a scanning methodology where scan direction is selected based on a determination of major and minor axes (*see*, for example, col. 4, lines 20-23). The scan axes are selected in response to an edge function, which determines whether a polygon to be rendered lies within a given tile (*see*, for example, col. 6, lines 13-67). Based on the results of the edge function, the resulting polygon is classified into one of several groupings (*see*, for example, FIG. 9-10 and col. 5, lines 31-44) and uses the resulting group value as an index to a look-up table (LUT), which provides the initial sampling point (*see*, for example, col. 5, lines 45-50). Thus, the location at which a raster engine initially scans, as disclosed in Wong, et al., is not based on generated "...region bits..." as defined in claim 1, but rather on a value contained in a LUT. In using the aforementioned method, the initial starting point will be located at one of the corners of the tile (*see*, for example, col. 5, lines 49-52), not within or substantially near the primitive to be rendered as defined in claim 1. Thus, Wong, et al. also does not teach or suggest the invention as defined in claim 1.

Consequently, as the combination of Aleksic and Lentz, et al. or Wong, et al. fails to teach or suggest the invention as defined in claim 1 or provide a motivation to combine the same, their combination cannot and does not render the invention as defined in claim 1 obvious. Accordingly, reconsideration of the rejection of claim 1 is respectfully requested.

Claim 2 depends upon and include all the limitations of claim 1 and are allowable at least for the reasons associated with claim 1. Accordingly, reconsideration of the rejection of claims 1-2 is respectfully requested.

C. Rejection of Claims 4-6

By this Amendment, claims 4-6 have been cancelled. Therefore, the rejection of those claims is rendered moot.

D. Rejection of Claims 7-17

(i) Claims 7-13

By this Amendment, claims 7-13 have been cancelled. Therefore, the rejection of those claims is rendered moot.

(ii) Claims 14-17

The Applicants traverse the rejection of these claims for the reasons set forth below. Claim 14 is an apparatus claim which defines a circuit which provides the initial rasterization starting point estimate according to the method of the present invention. As defined in claim 14, the inventive circuit of the present invention includes the following combination of components:

> "...a sorting circuit operative to provide sorted vertex data...in coordinate-dependent fashion, the vertex data including x-coordinate and y-coordinate position information;
>
> a region calculation circuit, coupled to the sorting circuit, operative to receive the sorted vertex data and to generate region bits representing the location of the sorted vertex data with respect to a current tile being rendered; and
>
> an initial rasterization starting point circuit, coupled to the region calculation circuit, operative to generate an initial rasterization starting point coordinate in response to the region bits, the initial rasterization starting point circuit including a discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the current tile."

Such combination of components is not taught or suggested by the combination of references as cited by the Examiner. As discussed in greater detail above in Section III(B), Aleksic is silent on how the initial scan point is generated. Lentz, et al. does not discuss, or is concerned with how the initial scan point is determined. Thus, the combination of Aleksic and Lentz, et al. does not render the first limitation of claim 14 obvious. In addition, Wong, et al. discloses that the initial rasterization starting point is based on information contained in an LUT as indexed by an edge function (*see*, for example, col. 6, lines 63-67), which does not depend upon, use or relate to region bits. A preliminary discussion of vertex data is disclosed, for example, at col. 7, lines 44-54; however, there is no disclosure within Wong, et al. as to whether such vertex information is "...sorted in coordinate-dependent fashion..." or subsequently used as defined in claim 14. Thus, as none of the references cited by the Examiner teach or suggest sorting input vertex data in coordinate-dependent fashion and the subsequent use thereof, the Applicants submit that the combination of references does not teach or suggest this limitation of claim 14.

In addition, none of the aforementioned references teaches or suggests the use or operation of a "...discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the current tile..." as defined in claim 14. More specifically, Aleksic and Lentz, et al. are silent on the use of a discard circuit. Wong, et al. does not disclose the use or operation of a discard circuit as the scanning of a primitive, or other suitable polygon, is started at the corner of a tile to be rendered (*see*, for example, col. 5, lines 49-50) and continues along both a major and a minor axes until the polygon to be rendered is located (*see*, for example, col. 7, lines 12-43). As such, because the scanning is defined as being performed within an entire tile, discarding is not performed. Consequently, as neither Aleksic, Lentz, et al. or Wong, et al. teaches or suggests the use or presence of a "...discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the current tile..." as defined in claim 14, the combination of such references also does not render this limitation obvious.

Consequently, as the combination of references cited by the Examiner does not teach or suggest at least two limitations of claim 14, such combination of references cannot and does not render the invention as defined in claim 14 obvious. Moreover, the combination of the aforementioned components that comprise the circuit of the present is also not taught or suggested by the combination of references; nor is there any motivation provided in any of the

cited references to make such a combination. Accordingly, reconsideration of the rejection of claim 14 is respectfully requested.

Claims 15-17 directly or indirectly depend upon and include all the limitations of claim 14 and are allowable at least for the reasons associated with claim 14. In addition, these claims define subject matter that is allowable over the art of record. For example, claim 15 provides a more detailed definition of the structure of the initial rasterization starting point circuit by introducing the "...trivial accept circuit..." component thereof and defining its corresponding functionality. It is respectfully submitted that the structure and functionality, for example, of the trivial accept circuit of claim 15 is not taught or suggested by the combination of references cited by the Examiner. Accordingly, reconsideration of the rejection of claims 14-17 is respectfully requested.

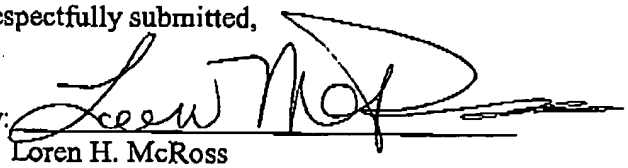
IV. New Claims

Claims 18-27 have been added to further introduce and define the inventive aspects and features of the present invention. For example, claims 18-22 and 24 define the structure and functionality of the interception calculation circuit and the trivial accept circuit, respectively. Claim 23 defines the structure and corresponding functionality of the discard circuit used in the initial rasterization starting point circuit of the present invention. Claims 25-26 define additional components that form the complete inventive circuit of the present invention and claim 27 is an independent claim which further defines the inventive circuit of the present invention. The Applicant's respectfully submit that these new claims are also allowable over the art of record.

Based on the above amendments and remarks, the Applicants submit that claims 1-3 and 14-27 are now in proper condition for allowance and such action is earnestly solicited.

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0441 for any payment in connection with this communication, including any fees for extension of time, which may be required. The Examiner is invited to call the undersigned if such action might expedite the prosecution of this application.

Respectfully submitted,

By: 

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Date: March 27, 2002

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Exhibit A

VERSION SHOWING CHANGES MADE

1. (Twice Amended) A method for providing an initial rasterizing point, comprising:

receiving vertex data corresponding to [first, second and third] the vertices of a [triangle] primitive, the vertex data including x-coordinate and y-coordinate position information;

sorting the vertex data in coordinate-dependent fashion;

generating region bits representing [a] the location [each] of the sorted vertex data [first, second and third vertices] with respect to a current tile being rendered;

generating coordinate data representing an initial rasterization starting point estimate [based in part on] when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered and discarding the sorted vertex data of primitives that lie outside the boundary of the current tile being rendered; and

providing the initial rasterization starting point estimate to a rasterizer.

2. (Twice Amended) The method of Claim 1, further comprising:

generating an orientation bit representing an orientation of a line connecting the first and second vertices of the sorted primitive with respect to a line connecting the first and third vertices of the sorted primitive before generating the initial rasterization starting point coordinates.

14. (Amended) A circuit, comprising:

a sorting circuit operative to provide sorted vertex data in response to input data corresponding to vertices of a primitive, the vertex data being sorted in a coordinate-dependent fashion, the vertex data including x-coordinate and y-coordinate position information;

a region calculation circuit, coupled to the sorting circuit, operative to receive the sorted vertex data and to generate region bits representing [a position of the primitive] the location of the sorted vertex data with respect to a current tile being rendered [in response to the sorted vertex data]; and

an initial rasterization starting point circuit, coupled to the region calculation circuit, operative to generate an initial rasterization starting point coordinate in response to the region bits, the initial rasterization starting point circuit including a discard circuit operative to discard

the vertex data of a primitive that lies outside the boundary defined by the [region bits] current tile.

15. (Amended) The circuit of Claim 14, wherein the initial rasterization starting point circuit further includes a trivial accept circuit operative to provide the actual coordinates of the primitive as the initial rasterization starting point in response to the region bits.